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Digitally Controlled Point of Load Converter with Very Fast Transient Response

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Abstract

This paper presents a new Digital Self-Oscillating Modulator (DiSOM) that allows the duty cycle to be changed instantly. The DiSOM modulator is shown to have variable switching that is a function of the duty cycle. Compared to a more traditional digital PWM modulator based on a counter and comparator the DiSOM modulator allows the sampling frequency of the output voltage control loop to be higher than the switching frequency of the power converter, typically a DC/DC converter. The features of the DiSOM modulator makes it possible to design a digitally controlled DC/DC converter with linear voltage mode control and very fast transient response.
The DiSOM modulator is combined with a digital PID compensator algorithm is implemented in a hybrid CPLD/FPGA and is used to control a synchronous Buck converter, which is used in typical Point of Load applications. The computational time is only three clock cycles from the time the A/D converter result is read by the control algorithm to the time the duty cycle command is updated.
A typical POL converter has been built and the experimental results show that the transient response of the converter is very fast. The output voltage overshoot is only 2.5% of the nominal output voltage when a load step of 50% - 100% of nominal output current is applied to the converter. The settling time is approximately 8 PWM cycles.

Introduction

Digital control of DC/DC converters has developed hugely over the past couple of years. By now digital control has emerged as a real alternative to traditional analogue control methods for DC/DC converters. Modern digital control techniques can meet the demands for fast transient response and accurate control of the output voltage as well as be cost competitive [1]. Several different solutions have been proposed to obtain fast dynamic response in a digitally controlled DC-DC converter, but the way they are implemented varies. The simplest way to implement digital control is to use voltage mode control with a linear compensation scheme [2-4]. The use of linear voltage mode control limits the obtainable control loop bandwidth for single phase DC-DC converters, because the sampling frequency is limited by the switching frequency of the converter. Reference [3] however shows that it is possible for a multiphase interleaved converter to obtain very high control loop bandwidth without increasing the switching frequency.
Another approach is to use digital current mode control [5-7] typically implemented as a predictive average current mode control scheme. Reference [5] presents a digital peak current mode control scheme, which works by sampling the inductor current at a sampling rate of 25MHz, which is very inhibitive in

terms of cost. Digital current mode control in general increases the complexity and thus the cost of the digital controller and does not necessarily lead to better transient responses for the DC-DC converter. Controllers mixing analogue and digital elements have also been proposed for high bandwidth digital control of DC-DC converters [8-9]. The results are promising but a mixed signal design will not lead to simpler system configuration and integrating both analogue and digital elements in one control IC will lead to higher production costs.

Non-linear control for DC-DC converters is another way to obtain fast dynamic response for DC-DC converters [10-11]. The proposed non-linear control scheme of ref. [10] relies on a non-uniform A/D converter, which is a cheap and easy solution with greatly improved dynamic performance. Reference [11] relies on a software implementation, where the control law is changed according to the output voltage error. The disadvantage of this is that the digital controller must perform a number of computations in order to decide which control law to use. This increases the cost of the controller as it has to run at a higher clock frequency, than a controller for a linear control scheme, to be able to sustain a sample rate equal to the sample rate of the linear control scheme.

Common for most of the above mentioned digital control solutions for DC/DC converter is that the PWM modulator is based on the traditional digital counter and comparator based implementation. This PWM modulator implementation imposes limitations on the digital controller implementation.

The problem of the digital PWM modulator is the basic design, which is based on a counter and a comparator. The issue is that the counter counts from zero to a preset value and the counter value is compared to the duty cycle register, which is set by the digital control law, e.g. a PID compensator. The PWM output is high when the counter value is lower than the duty cycle register and changes to low when the counter value exceeds the duty cycle register. The duty cycle register is latched in order to avoid unwanted changes on the PWM output, and the latch is enabled/updated when the counter is reset to zero. Depending on the sampling scheme, i.e. the time the output voltage is sampled in relation to the PWM signal, the delay from the time when the output voltage is sampled to the time when the duty cycle register is updated can be up to one PWM period in state-of-the-art digital control solutions. The time delay results in negative phase shift, which will limit the control loop bandwidth. The update rate of the duty cycle register is limited to once per switching period independent of the sampling scheme.

Most systems sample the output voltage at the beginning of a PWM period and the resulting new duty cycle is latched into the duty cycle register for the following PWM period [2]. In this case the computational delay of the digital controller is not very important as long as it can calculate the new duty cycle during one PWM period. New modulators for multiphase interleaved converters have been proposed that allows the sampling frequency of the output voltage control loop to be higher than the single phase PWM frequency [3]. In this case the computational delay of the digital control algorithm becomes the limiting factor for the control loop bandwidth.

A new digital modulator called a Digital Self-Oscillating Modulator (DiSOM) is presented in this paper along with a digital PID compensator with very short computational delay. An advantage of the DiSOM modulator over counter based PWM modulators is that the duty cycle register can be updated at any instant in time without unwanted shifts on the PWM output. This feature of the DiSOM allows the use of linear control for a DC-DC converter with very fast transient response.

Digital Self-Oscillating Modulator

The DiSOM modulator described in this paper is just one of a family of modulators that are included in a new invention described in reference [14]. The DiSOM modulator (see Fig. 1) is a self-oscillating modulator with a local feedback loop placed around the switching output. The modulator consists of a comparator with hysteresis, a feedback block (MFB) and a forward block (MFW). In this implementation of the DiSOM modulator the feedback block is a simple multiplication/gain but it could also be a digital filter if advantageous. The forward block is a digital integrator and the output of the integrator, also called the carrier, will be a triangular waveform under steady state conditions. The "*Ref*" input defines the duty cycle of the switching output because it affects the slope of the carrier.

One disadvantage of the DiSOM modulator is that the switching frequency changes with the duty cycle. The switching frequency as a function of the duty cycle command is a parabolic function, which goes to zero for duty cycles equal to 0 and 1. A mathematical derivation of the switching frequency as a function of the duty cycle is derived in the following subparagraph.
Fig. 2 shows a simulated example of the transient response of the DiSOM modulator to a change on the reference input, "*Ref*". The reference input is changed from 0.8 to 0.2 in the middle of a switching period at $t = 7.5\mu s$. The output of the DiSOM change from high to low almost immediately after the reference input is changed and the new duty cycle can be observed after $t = 8.0\mu s$. This ability to change the duty cycle in the middle of a switching period allows the control system to react faster to transient conditions, such as a load step.

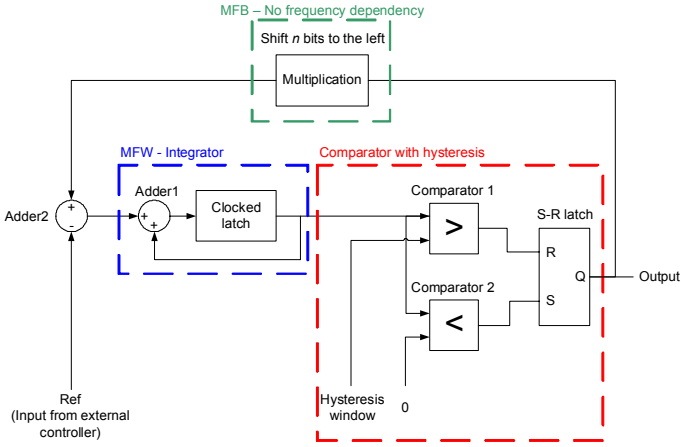

Fig. 1: Block diagram of the DiSOM modulator

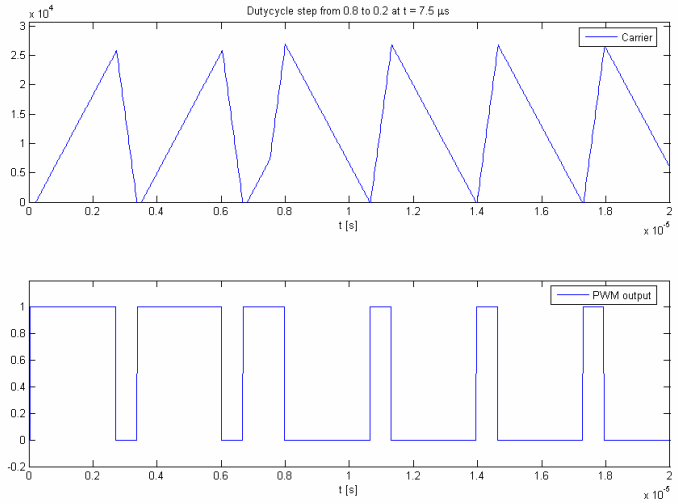

Fig. 2: Duty cycle change from 0.8 to 0.2 for the DiSOM modulator

Derivation of the switching frequency versus duty cycle for the DiSOM modulator

The switching frequency of the DiSOM modulator of Fig. 1 can be derived from a time domain analysis of the system. Fig. 3 shows the internal signals of the DiSOM modulator. The mathematical expression for the switching frequency is derived without taking into account the discrete time nature of the DiSOM modulator. That means that it is assumed that the carrier will oscillate between 0 and the hysteresis window, *Window*, without exceeding either limit due to clock frequency quantization.

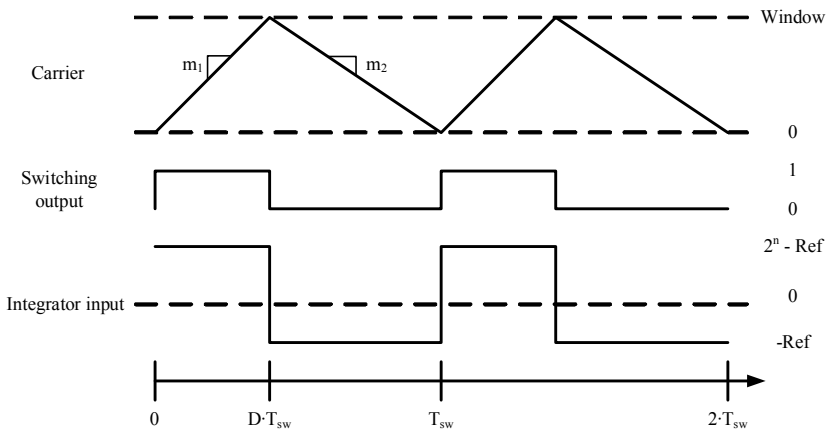

Fig. 3. Internal signals of the DiSOM modulator

The slopes of the carrier m_1 and m_2 depend on the integrator input and the clock frequency of the system (see equation (1) and (2)). The variable n is the number of bits used to represent the reference input, *Ref*, in the digital implementation of the DiSOM modulator and f_{clock} is the clock frequency.

$$m_1 = \left(2^n - Ref\right) \cdot f_{clock} \tag{1}$$

$$m_2 = -Ref \cdot f_{clock} \tag{2}$$

During the ON period of the switching output the carrier will change from *0* to *Window* and during the OFF period it will return to 0. The switching frequency is calculated by equating the ON time of the switching signal with the change in the carrier signal during the ON time as expressed in equation (3).

$$D \cdot T_{sw} = \frac{Carrier\left(T_{sw}\right) - Carrier\left(0\right)}{m_1} = \frac{Window}{\left(2^n - Ref\right) \cdot f_{clock}} \tag{3}$$

Finally by inserting the relationship between the reference input, *Ref*, and the duty cycle, *D*, (see equation (4)) into the expression for the switching frequency it is possible to derive a mathematical expression for the switching frequency as a function of the duty cycle (see equation (5)).

$$D = \frac{Ref}{2^n} \tag{4}$$

$$f_{sw}\left(D\right) = \frac{2^n \cdot f_{clock}}{Window} \cdot \left(D - D^2\right) \tag{5}$$

Digital controller implemented in a Hybrid FPGA/CPLD

A special digital PID compensator has been designed in VHDL and implemented in a hybrid CPLD/FPGA (LCMXO1200C) from Lattice semiconductor. The computational delay of the PID algorithm is nine clock cycles from the instant of sampling the output voltage to the time the duty cycle input of the DiSOM is updated. The digital PID controller is implemented with the specific purpose of working as a PID controller and it can not easily be changed. The advantage of the implemented PID compensator compared

to a more conventional Digital Signal Processor (DSP) implementation [12] is that because it is specifically designed as a PID compensator, it can be optimized to give as short a computational delay as possible. In this way the complexity of the digital hardware can be optimized as well.
A principal block diagram of the PID compensator is shown in Fig. 4. The Digital PID compensator is implemented using a lookup table stored in non-volatile memory rather than with a multiplier/accumulator structure as known from DSPs. The digital PID compensator has the discrete time transfer function of equation (6) and the digital implementation must calculate the result of a difference equation (equation (7)) in order to implement the PID compensator.

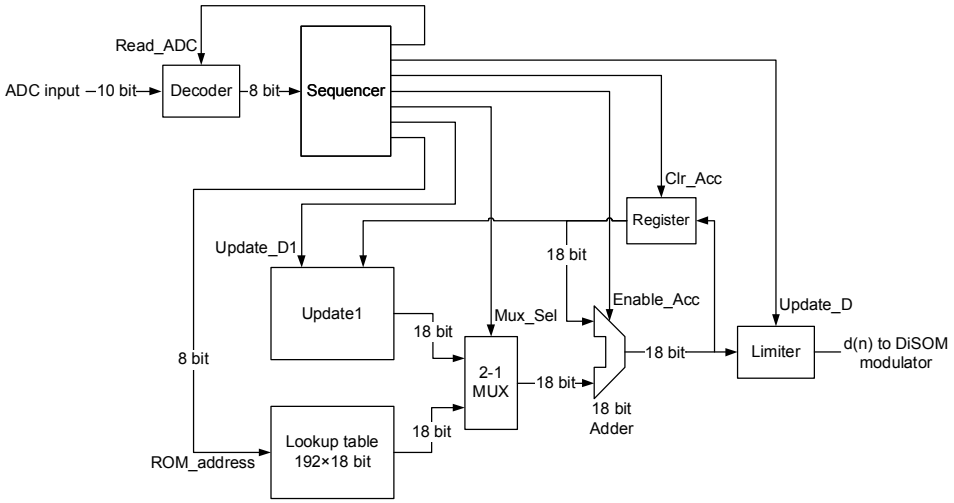

Fig. 4: Block diagram of digital PID compensator implementation in the FPGA

$$G_{PID}(z) = \frac{d(z)}{e(z)} = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^{-1}} \tag{6}$$

$$d(n) = d(n-1) + b_0 \cdot e(n) + b_1 \cdot e(n-1) + b_2 \cdot e(n-2) \tag{7}$$

where b_0, b_1 and b_2 are constant coefficients, d is the duty cycle command, e is defined as the difference between the output voltage reference and the measured output voltage and n is the sample number.
A short functional description of each block in Fig. 4 is given below:

- Sequencer – The sequencer is a state machine that controls the timing of the digital PID compensator. A counter clocked by the system clock is counting from 0 to 63 and is used to define the states. The control signals for the other blocks of the PID compensator are defined for each state. A timing diagram for the operation of the PID compensator is shown in Fig. 5.
- Decoder – The Decoder takes the A/D converter (ADC) result, which is 10 bit wide, and calculates the appropriate address for the lookup table for the error *e(n)*. The ADC result is 10 bits because a 10 bit ADC is mounted on the FPGA development board but the error is reduced to 6 bits in order to reduce the size of the lookup table. The Read_ADC signal from the Sequencer commands the Decoder to update the 8-bit address based on the current ADC result.
- Lookup Table – The Lookup Table holds the results of the multiplication of *e(n)*, *e(n-1)* and *e(n-2)* by b_0, b_1 and b_2 respectively. The Lookup Table has an 8-bit address input in order to address the 192 positions in the table. That is 64 positions for each error signal, i.e. *e(n)*, *e(n-1)* and *e(n-2)*. The result of each multiplication is 18 bits wide and the five least significant bits are used to represent fractions of 1. That means that each of the coefficients b_0, b_1 and b_2 can be adjusted in

steps of 1/32 (0.03125) and the coefficients can take on values in the range of -64 to +64. The Lookup Table is stored in a special memory area of the FPGA and takes up 432 bytes of memory.

- Update1 – Update1 takes the duty cycle calculated as *d(n)* and stores it for use as *d(n-1)* for the next run of the PID algorithm. Update1 also limits the duty cycle to the range from 0 to 1, so that internal overflow can not occur in the compensator. Update1 is controlled by the Update_D1 signal.
- 2-1 MUX – This is a two input multiplexer, which is used to select if the output of either Update1 or the Lookup Table is fed to the Accumulator. The multiplexer is controlled by the Mux_sel signal.
- Accumulator – The Accumulator is composed of the 18-bit Adder and the Register. The Register holds the result of the Accumulator and is connected to one input of the adder. The Accumulator can be cleared by the setting the Clr_Acc signal high and enabled by setting Enable_Acc high.
- Limiter – The Limiter has two functions. The first is to limit the duty cycle from approximately 0.01 to 0.99 and the other is to reduce the 18 bit result of the Accumulator to a 10 bit representation for the DiSOM modulator. The output of the Limiter is updated by pulling Update_D high.

The timing diagram of Fig. 5 shows that the Read_ADC signal is asserted at state no. 4 and the Update_D signal is asserted state no.7. This corresponds to a delay of three clock cycles but the total delay of the actual implementation is nine clock cycles as already stated. The extra delay is due to the choice of ADC, which for the FPGA development board is a 10 bit pipelined ADC. The pipelined ADC has 5 pipeline stages resulting in a total sampling delay of 6 clock cycles. The ADC is running on the same clock as the FPGA and the thus the total delay, i.e. sampling + computational delay, is nine clock cycles. If a flash ADC had been used instead, the total delay could be reduced to four clock cycles reducing the negative phase shift caused by the delay even further.
The ROM_address signal takes on three values (Address0, Address1 and Address2) during the computation of the duty cycle. The three addresses refer to each of the three values that must be read from the lookup table. Address0 refers to the present error, *e(n)*, Address1 to the previous error *e(n-1)*, and Address2 to the error of two samples previously, *e(n-2)*.

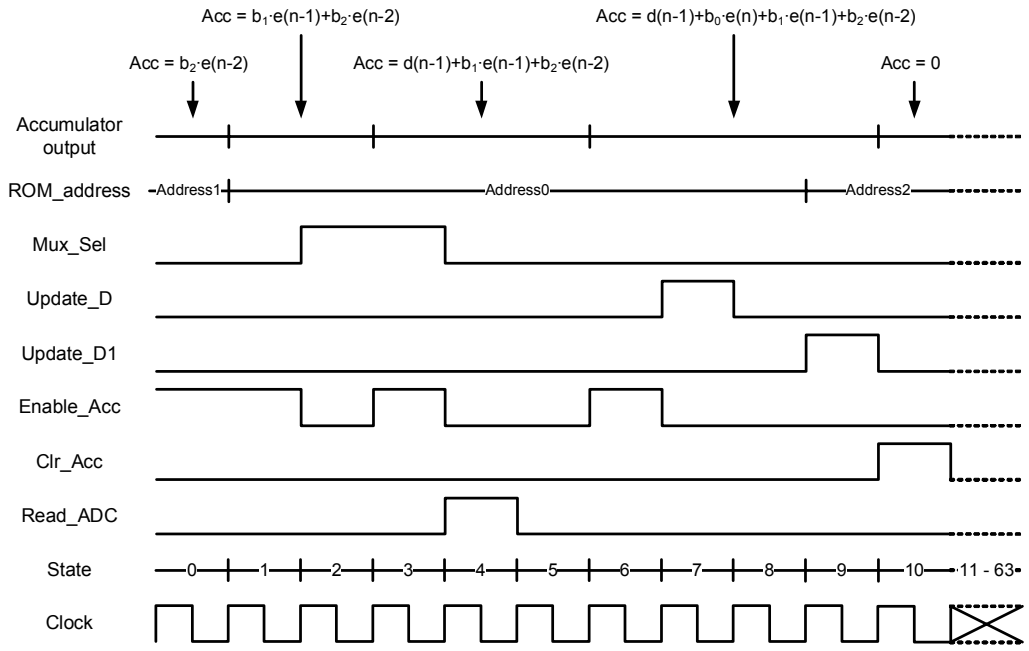

Fig. 5: Timing diagram for the digital PID compensator implementation

The total computation time is eleven clock cycles and the maximum sampling frequency is limited to one eleventh of the clock frequency. This is due to the fact that delays have to be inserted in the algorithm because of the need for pipelining signals in the FPGA. The time it takes to complete the algorithm could be reduced further by using a parallel implementation of the PID compensator as proposed in ref. [13]. A parallel implementation does on the other hand increase the complexity and price of the digital control solution and in most cases it will not be necessary to run at very high sampling frequencies.

Experimental results

A Buck converter with synchronous rectification has been built and tested together with DiSOM modulator and digital PID compensator blocks implemented in the Lattice Semiconductor LCMXO1200C CPLD/FPGA and with the ADC10065 ADC from National Semiconductor. The specifications for the Buck converter and control scheme are given in Table I and the specifications for the digital implementation of the DiSOM modulator and PID compensator are given in Table II. The output capacitance is four 100µF ceramic capacitors in parallel to achieve as low equivalent series resistance and inductance as possible. The Buck converter design has been optimized for efficiency since the purpose of the design was to prove the feasibility of the proposed digital controller.
A picture of the experimental setup is shown in Fig. 6, where the FPGA development board is on the left and the Buck converter PCB is on the right. Fig. 7 shows a block diagram of the prototype setup.

Table I: Prototype specifications

Parameter	Value
Input voltage	9 – 15 V
Output voltage	2.0 V
Output current	0 – 10 A
Inductor size	1.5 µH
Output capacitance	400 µF
Output capacitance ESR	<2 mΩ
Nominal switching frequency @ D = 0.5	625 kHz

Table II: Specifications for the digital controller

Parameter	Value
Clock frequency	50MHz
Reference input resolution	10 bit
Hysteresis window	20480
Effective ADC resolution	6 bit
Effective ADC range	1.419 – 1.481V
Sampling frequency	800 kHz

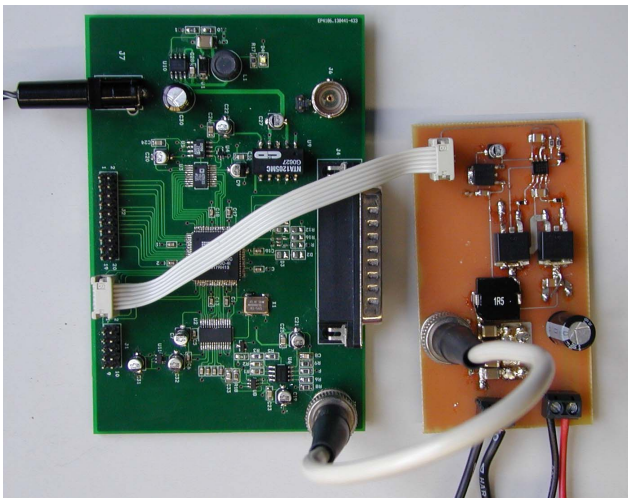

Fig. 6: The experimental setup. FPGA/CPLD board on the left and Buck converter PCB on the right

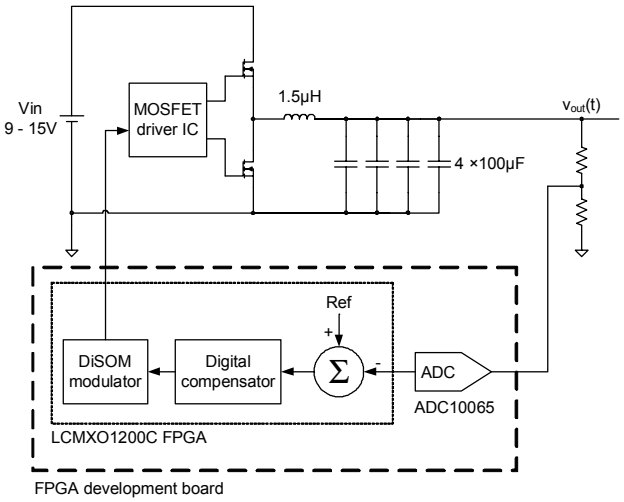

Fig. 7: Block diagram of the prototype setup

The digital PID compensator transfer function for the prototype design is given in equation (8).

$$G_c(z) = \frac{12.8125 - 22.6875 \cdot z^{-1} + 9.9375 \cdot z^{-2}}{1 - z^{-1}} \tag{8}$$

Fig. 8 shows the theoretical and measured open loop Bode plots for the prototype. The computational delay of the digital PID controller has been included in the theoretical small signal model of the system, so the two Bode plots are comparable. The prototype has a phase margin of 60 degrees and a crossover frequency of 37 kHz. The gain margin is 22 dB at 151 kHz. At frequencies higher than the crossover frequency the prototype has more negative phase shift than the model, which is probably due to the fact that the DiSOM modulator will have a delay of one or two clock cycles which hasn't been included in the model. The resonant peak at the output filter resonance frequency is not apparent in the experimental measurement, which is not easily explained. One explanation could be that the Gain/Phase analyzer, used to measure the Open loop transfer function, increased the test frequency in too large steps around the resonant frequency, thereby missing the resonant peak.

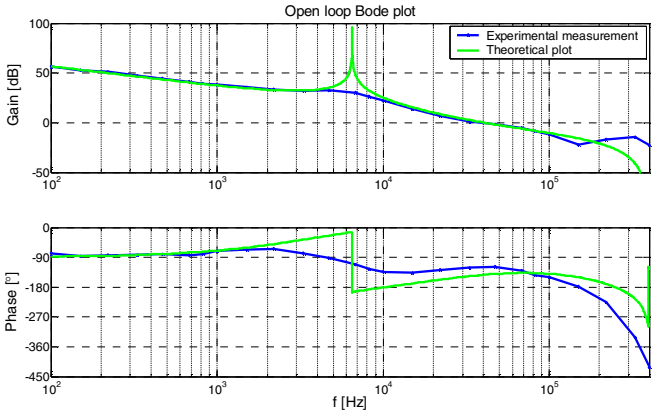

Fig. 8: Theoretical and measured open loop Bode plots

The transient response to a 50% load step has been measured for both positive and negative load steps, see Fig. 9. The upper trace is the output voltage with the oscilloscope AC coupled (20mV/div) and the lower trace is the output current (5A/div). The time scale of the measurements is 10µs/div. During the load step

the output current has a rate of change of approximately 1A/µs, which was limited by the electronic load used in the experiment. Simulations have shown that the converter performs almost as well if the rate of change is 100A/µs. The output voltage overshoot is 50 mV, which is 2.5% of the nominal output voltage and the settling time is approximately 20 µs.

Fig. 10 is a measurement of the output during steady state conditions. The upper trace is the output voltage (AC coupled 10mV/div) and the lower trace is the output current (5A/div). The trace in the middle shows the switch node voltage of the Buck converter (10V/div) and it shows that the switching frequency is a little below 500 kHz at nominal output current. The output voltage has a non-periodic limit cycle with an amplitude of 12 mV or 0.6% of the nominal output voltage. The limit cycling can to a certain extent be explained by the fact that the ADC measurement is disturbed by switching noise. It is however also attributable to the fact that the output voltage is sampled at faster rate than switching frequency and with a very high resolution, which means the output voltage ripple is sampled and fed through the digital compensator. This will disturb the PWM signal generated by the DiSOM and may cause the output voltage to limit cycle.

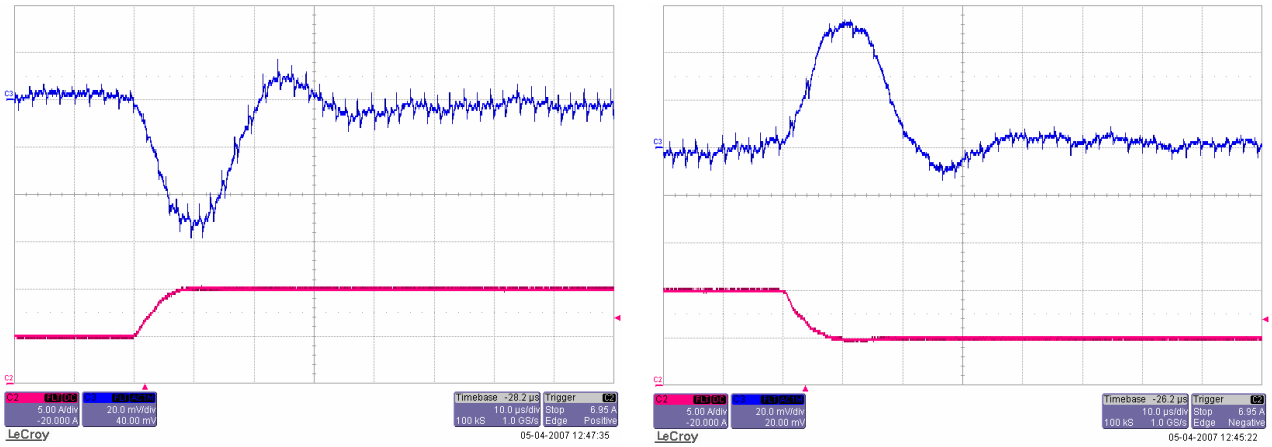

Fig. 9: Positive load step from 5A to 10A (V_{in} = 12V).
Upper trace: V_{out} 20mV/div, Lower trace: I_{out} 5A/div, Time scale: 10µs/div

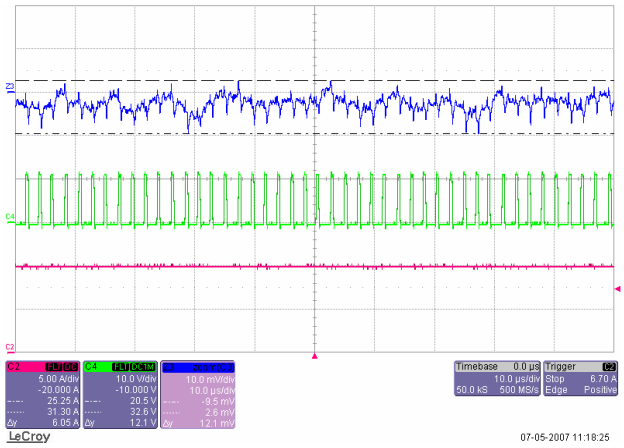

Fig. 10: Limit cycling on the output voltage (V_{in} = 12V, I_{out} = 10A). Upper trace: V_{out} 10mV/div
Middle trace: Switch node 10V/div, Lower trace: I_{out} 5A/div, Time scale 10µs/div

Conclusion

A new Digital Self-Oscillating Modulator (DiSOM) based on a local feedback loop around the switching output has been presented. The duty cycle command of the DiSOM modulator can be updated at any

instant in time irrespective of the state of the output. This gives the DiSOM modulator the ability to change its duty cycle at any time and makes it possible for a linear control loop to sample the output voltage at a higher rate than the switching frequency thereby enabling higher control loop bandwidth.It has been shown that the switching frequency of the DiSOM modulator is a parabolic function with maximum switching frequency at a duty cycle of 0.5 and going towards zero for duty cycles equal to 0 or 1.

A digital PID compensator has been implemented in a hybrid CPLD FPGA, resulting in a computational delay of just three clock cycles between availability of the ADC result and the following update of the duty cycle command. The total delay from the instant the output voltage is sampled until the duty cycle command is updated is nine clock cycles because a pipelined ADC was used.

The DiSOM modulator and digital PID controller have been combined in a digital controller for a low voltage synchronous Buck converter. The experimental results show that the converter has high control loop bandwidth and very fast transient response. For a load step from 50% to 100% of nominal output current the output voltage overshoot is 2.5% of nominal value and the settling time is equal to approximately eight switching cycles.

There is some non-periodic limit cycling on the output but it is mainly caused by noise on the output voltage that disturbs the control loop. The limit cycling is approximately 0.6% of nominal output voltage.

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